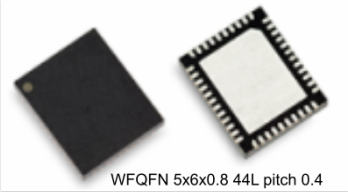
STPMIC1

Data brief

14 output rail PMIC, 4 COT high performance buck SMPS, BOOST with bypass, LDO for memory power supply


WFQFN 5x6x0.8 44L pitch 0.4

Features

- Large input voltage range from 2.8 V to 5.5 V
- 4 adjustable general purpose LDOs
- 1 LDO for DDR3 DDR3 termination (sink-source) or bypass mode for lpDDR or general purpose
- 1 LDO for USB PHY supply with automatic power source detection
- 1 reference voltage LDO for DDR memory
- 4 adjustable adaptive constant on-time (COT) buck SMPS converters
- 5.2 V / 1.1 A boost SMPS with bypass mode for 5 V input or battery input
- 1 power switch 500 mA USB OTG compliant
- 1 power switch 500 mA/1000 mA general purpose
- User programmable non-volatile memory (NVM), enabling scalability to support a wide range of applications
- I²C and digital IO control interface
- WFQFN 5x6x0.8 44 leads

Applications

- Integrated PMU for complete MPU applications
- eReaders, weareable, IoT
- Portable devices
- Man-machine interfaces
- Home automation
- System on-module

Product status link
STPMIC1

Device summary	
Marking	STPMIC1A
	STPMIC1B
	STPMIC1C
Packing	WFQFN 5x6x0.8 44 leads

Description

The STPMIC1 is a fully integrated power management IC designed for products based on high integrated application processor designs requiring low power and high efficiency.

The device integrates advanced low power features controlled by a host processor via I²C and IO interface.

The STPMIC1 regulators are designed to supply power to the application processor as well as to the external system peripherals such as: DDR, Flash memories and other system devices.

The boost converter can power up to 3 USB ports (two 500 mA host USB and one 100 mA USB OTG). Its advanced bypass architecture allows smooth regulation of VBUS for USB ports from a battery as well as low-cost consumer 5 V AC-DC adapters.

4 buck SMPS are optimized to provide excellent transient response and output voltage precision for wide range of operating conditions, high full range efficiency (η up to 90%) by implementing low power mode with smooth transition from PFM to PWM and also advanced PWM synchronization technique with integrated PLL for better noise/EMI performance.

1 Device configuration table

The STPMIC1 has a non-volatile memory (NVM) that enables scalability to support a wide range of applications:

- Default output voltage, POWER_UP/POWER_DOWN sequence, protection behavior, auto turn-on functionality, I^2C slave address
- The STPMIC1A and STPMIC1B are pre-programmed part number to support the all STM32MP1 series application processor versions
- The STPMIC1C is not programmed part number to support custom applications
- Straightforward NVM (re)programming via I^2C to facilitate mass production directly in target applications
- Possibility to lock NVM content to prevent further re-programming by writing LOCK_NVM bit

Table 1. Default NVM configuration vs part number

	Default configuration table					
	STPMIC1A		STPMIC1B		STPMIC1C	
	Default output voltage	Rank	Default output voltage	Rank	Default output voltage	Rank
LDO1	1.8 V	0	1.8 V	0	1.8 V	0
LDO2	1.8 V	0	2.9 V	2	1.8 V	0
LDO3	1.8 V	0	1.8 V	0	1.8 V	0
LDO4	3.3 V	3	3.3 V	3	3.3 V	0
LDO5	2.9 V	2	2.9 V	2	1.8 V	0
LDO6	1.0 V	0	1.0 V	0	1.0 V	0
REFDDR	0.55 V	0	0.55 V	0	0.55 V	0
BOOST	5.2 V	N/A	5.2 V	N/A	5.2 V	N/A
BUCK1	1.2 V	2	1.2 V	2	1.1 V	0
BUCK2	1.1 V	0	1.1 V	0	1.1 V	0
BUCK3	3.3 V	1	1.8 V	1	1.2 V	0
BUCK4	3.3 V	2	3.3 V	2	1.15 V	0
	Default value					
VINOK_Rise	3.5 V		3.3 V		3.5 V	

The start-up sequence is split into four steps (Rank0 to Rank3).

Each BUCK converter or LDO regulator can be programmed to be automatically turned ON in one of these phases:

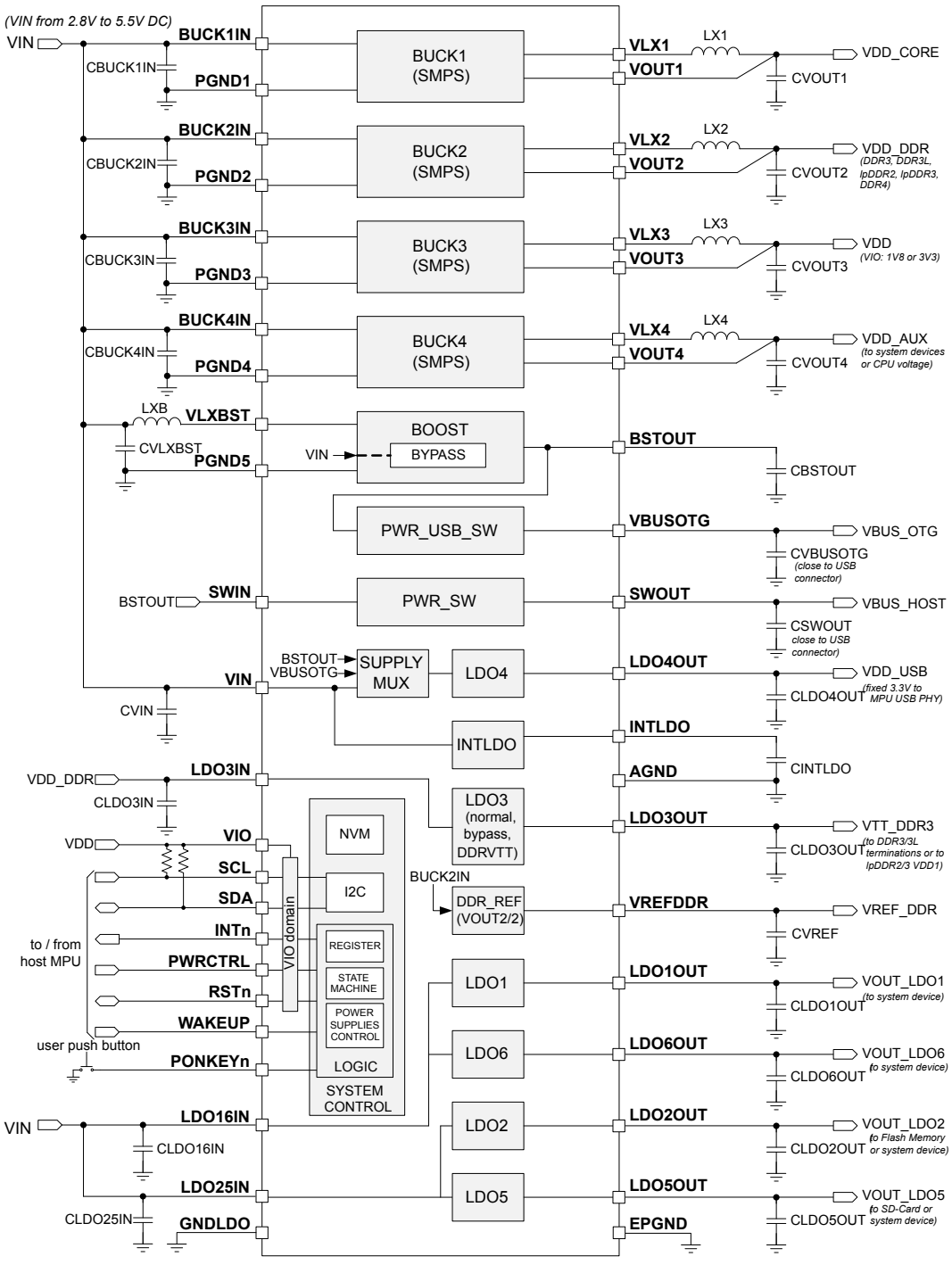
- Rank= 0: rail not turned ON automatically, no output voltage appears after POWER-UP
- Rank= 1: rail automatically turned ON after 3 ms
- Rank= 2: rail automatically turned ON after further 3 ms
- Rank= 3: rail automatically turned ON after further 3 ms

Whatever STPMIC1x version:

- AUTO_TURN_ON option is set
- Boost and switches cannot be turned ON automatically

2 Typical application schematic

Figure 1. **Typical application schematic**



Note: BUCK1IN and BUCK2IN must always be connected to VIN

3 Recommended external components

Table 2. Passive components

Component	Manufacturer	Part number	Value	Size
CVIN, CLDO1OUT, CLDO2OUT, CLDO4OUT, CLDO5OUT, CLDO6OUT, CINTLDO	Murata	GRM155R60J475ME47#(1)	4.7 µF	0402
CVLXBST, CBUCK1IN, CBUCK2IN, CBUCK3IN, CBUCK4IN, CLDO3IN, CLDO3OUT(2)		GRM188R61A106KE69D	10 µF	0603
CLDO16IN, CLDO25IN, CVREF		GRM155R61E105KA12	1 µF	0402
CVBUSOTG		GRM188R61C475KE11#	4.7 µF	0603
CBSTOUT, CVOUT1, CVOUT2, CVOUT3, CVOUT4		GRM188R60J226MEA0	22 µF	0603
CSWOUT		GRM31CR60J227ME11L	220 µF	0603
LX1, LX2, LX3, LX4, LXB		DFE252012P-1R0M=P2	1 µH	1008

1. *# is the last P/N digit; it indicates a package specification code.*
2. *4.7 µF normal mode - 10 µF sink/source mode - no cap bypass mode.*

Note: all the above components refer to a typical application. Operation of the device is not limited to the choice of these external components.

4 Power regulators and switch description

4.1 Overview

The STPMIC1 has large input voltage range from 2.8 V to 5.5 V to supply application from typically 5 V DC wall-adaptor or from 1-cell 3.6 V Li-Ion / Li-PO battery or from USB port (bus-powered).

The STPMIC1 provides all regulators needed to power supply a complete application:

- 6 LDOs + 1 reference voltage LDO for DDR memories
- 4 step-down (buck) converters
- 1 step-up (boost) converter with bypass to supply USB sub-system
- 2 power switch to supply USB sub-system

Table 3. General description

Regulator	Output voltage (V)	Programming step(mV)	Rated output current (mA)	Application use (example)
LDO1	1.7 to 3.3	100	350	GP
LDO2	1.7 to 3.3	100	350	SD-card or GP
LDO3 normal mode	1.7 to 3.3	100	100	lpDDR_1V8 or GP
LDO3 sink/source mode	VOUT2 / 2 (BUCK2)	-	+/-120 (+/-200 peak)	DDR3 VTT (termination)
LDO3 bypass mode	LDO3IN-V_{DROP_LDO3}	-	50	lpDDR_1V8
LDO4	3.3 (fixed)	-	50	USB PHY
LDO5	1.7 to 3.9	100	350	Application FlashMem or GP
LDO6	0.9 to 3.3	100	150	GP
REFDDR	VOUT2 / 2 (BUCK2)	-	+/-5	Vref DDR
BUCK1	0.725 to 1.5	25	1500	Application CORE
BUCK2	1 to 1.5	50	1000	lpDDR2/3/4, DDR3/L, DDR4
BUCK3	1 to 3.4	100	500	Application VIO
BUCK4	0.6 to 3.9	25 (0.6 V to 1.3 V) 50 (1.3 V to 1.5 V) 100 (1.5 to 3.9 V)	2000	Application CPU or GP
BOOST	5.2 V (fixed)	-	1100	USB ports
VBUSOTG_SW	~BSTOUT	-	500	USB OTG/DRD
PWR_SW	~SWIN	-	1000	USB or GP

LDO1, LDO2, LDO5, LDO6 are general purpose (GP) LDO (low-dropout) linear regulators and can be used to supply application peripherals.

LDO3 is a multipurpose linear regulator that support 3 modes:

- **Normal mode**: operates as standard LDO with 1.7 to 3.3 V output voltage range (for general purpose use)
- **Sink/source mode**: LDO3 operates in sink/source regulation mode to supply termination resistors of DDR3/DDR3L memory interface (VTT voltage)

- **Bypass mode**: LDO3 operates as simple power switch to supply lpDDR2/3 VDD1 (1.8 V) power domain. In that case, LDO3IN is supplied from 1.8 V. This is a preferred mode versus normal mode in term of power efficiency to power supply lpDDR2/3 VDD1

LDO4 is a fixed output voltage (3.3 V) LDO and is dedicated to power supply host processor USB PHY. It is able to automatically switch between 3 power inputs (VIN, VBUSOTG and BSTOUT) to provide valid output voltage in all application use cases, for example to support discharged battery for Li-Ion/Li-PO battery-powered device

DDR REF is sink/source reference voltage LDO dedicated to power VREF of lpDDR/DDR.

BUCK1 to BUCK4 are 2 MHz synchronous step-down converters optimized for high efficiency. To improve transient response, converters use adaptive constant on-time (COT) controller with a nominal switching frequency of 2 MHz.

In low power (LP) mode converters operate in hysteretic mode to minimize quiescent current and improve efficiency while still keeping excellent transient response.

Buck controller also support dynamic voltage scaling (DVS) capability with active discharge (voltage tracking) and switching phase shifting pi/2 mutual synchronization between converters for reducing switching EMI radiation.

BOOST is a fixed output voltage 5.2 V step-up converter dedicated to power supply USB ports (VBUSOTG_SW and/or PWR_SW power switches). In addition to support step-up conversion for battery applications (to convert VBAT=3.6 V to VBUS= 5.2 V), this boost converter has been enhanced with a special bypass circuitry with smooth output voltage transitions to comply USB VBUS tolerance when application is powered from commonly available 5 V wall adaptors. This is to compensate voltage tolerance of voltage source (wall adaptor) and voltage drop through the PCB from input supply of device to USB port.

VBUSOTG_SW is a 500 mA power switch suitable for USB OTG port or USB Type-C DRD. Input is internally connected to BOOST output. It supports VBUS detection, OCP and reverse current protection.

PWR_SW is a 1000 mA power switch, that can supply max. 2 USB STD HOST port or for general purpose.

5 Pinout and pin description

Figure 2. **Pin configuration WFQFN 44 leads top view**

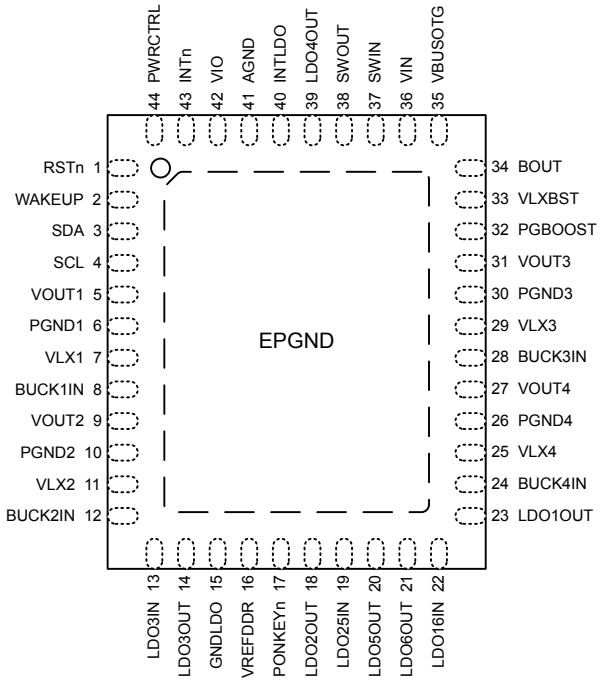


Table 4. **Pin description**

Pin name	A/D[1]	I/O	Location	Description (default configuration)
RSTn	D	I/O	1	Bi-directional reset (active low with internal pull-up)
WAKEUP	D	I	2	Power-ON from host processor (active high with internal pull-down)
SDA	D	I/O	3	I^2C serial data
SCL	D	I	4	I^2C serial clock
VOUT1	A	I	5	Input feedback signal buck converter 1
PGND1	A	-	6	Power ground buck converter 1
VLX1	A	O	7	LX node buck converter 1
BUCK1IN	A	I	8	Power input buck converter 1
VOUT2	A	I	9	Input feedback signal buck converter 2
PGND2	A	-	10	Power ground buck converter 2
VLX2	A	O	11	LX node buck converter 2
BUCK2IN	A	I	12	Power input buck converter 2
LDO3IN	A	I	13	Power input LDO3
LDO3OUT	A	O	14	Output voltage LDO3
GNDLDO	A	-	15	LDO GND
VREFDDR	A	O	16	DDR VREF output voltage

Pin name	A/D[1]	I/O	Location	Description (default configuration)
PONKEYn	D	I	17	User power ON key (active low with internal pullup)
LDO2OUT	A	O	18	Output voltage LDO2
LDO25IN	A	I	19	Power input LDO2 and LDO5
LDO5OUT	A	O	20	Output voltage LDO5
LDO6OUT	A	O	21	Output voltage LDO6
LDO16IN	A	I	22	Power input LDO1 and LDO6
LDO1OUT	A	O	23	Output voltage LDO1
BUCK4IN	A	I	24	Power input buck converter 4
VLX4	A	O	25	LX node buck converter 4
PGND4	A	-	26	Power ground buck converter 4
VOUT4	A	I	27	Input feedback signal buck converter 4
BUCK3IN	A	I	28	Power input buck converter 3
VLX3	A	O	29	LX node buck converter 3
PGND3	A	-	30	Power ground buck converter 3
VOUT3	A	I	31	Input feedback signal buck converter 3
PGND5	A	-	32	Power ground boost converter
VLXBST	A	I	33	LX Node boost converter
BSTOUT	A	O	34	Output voltage boost converter
VBUSOTG	A	O	35	Power output switch powered by boost converter
VIN	A	I	36	Main power input - power input LDO4, VREF
SWIN	A	I	37	Power input switch
SWOUT	A	O	38	Power output switch
LDO4OUT	A	O	39	Output voltage LDO4
INTLDO	A	O	40	Internal LDO
AGND	A	-	41	Main analog ground
VIO	A	I	42	I/O voltage (for all digital signals except WAKEUP and PONKEYn)
INTn	D	O	43	Interrupt (active low with internal pull-up)
PWRCTRL	D	I	44	Power control mode (pull-up and pull-down inactive by default)
EPGND	A	-	ePad	Exposed pad to be connected to ground

1. *A: analog; D: digital*

Revision history

Table 5. **Document revision history**

Date	Version	Changes
06-Feb-2019	1	Initial release.